SESSION 11 – TAPA II
High k Dielectric Technology

Wednesday, June 16, 10:20 p.m.
Chairpersons: R. Chau, Intel
M. Niwa, Matsushita Electric

11.1 — 10:20 a.m.

Performance and Reliability of Sub-100nm TaSiN Metal Gate Fully-depleted SOI Devices with High-K (HfO_2) Gate Dielectric, A.V-Y. Thean, A. Vandooren, S. Kalpat, Y. Du, I. To, J. Hughes, T. Stephens, B. Goolsby, T. White, A. Barr, L. Mathew, M. Huang, S. Egley , M. Zavala, D. Eades, K. Sphabmixay*, J. Schaeffer, D. Triyoso, M. Rossow, D. Roan, D. Pham, R. Rai, S. Murphy, B.-Y. Nguyen, B. E. White, A. Duvallet, T. Dao and J. Mogab, Motorola, Inc., Austin, TX, *STMicroelectronics, Austin, TX

We report the performance and reliability of sub-100nm TaSiN metal gatefully-depleted SOI devices with high-k gate dielectric. Performance differences between fully-depleted and partially-depleted devices are highlighted. It is also the first time that an unique asymmetric degradation between electron and hole mobility in metal/high-k devices is reported. Despite the use of high-k dielectric, we show that these devices exhibit superior reliability, noise and analog circuit performances.

11.2 — 10:45 a.m.

Physics in Fermi Level Pinning at the PolySi/Hf-based High-k Oxide Interface, K. Shiraishi, K. Yamada*, K. Torii**, Y. Akasaka**, K. Nakajima^, M. Kohno^^, T. Chikyo^, H. Kitajima**, and T. Arikado**, University of Tsukuba, Tsukuba, Japan, ^National Research Institute of Materials Science, Tsukuba, Japan, *Waseda University, Tokyo, Japan, **Semiconductor Leading Edge Technologies, Inc., Tsukuba, Japan, ^^Hitachi Science Systems, Ltd., Hitachi-Naka, Japan

We report that O vacancy (Vo) formation in ionic Hf-based dielectrics and subsequent electron transfer into poly Si gates across the interface, definitely cause substantial flat band (Vfb) shifts especially for p+ gate MISFETs. Our theory can systematically reproduce experiments related to Hf-based dielectrics, and gives a guiding principle towards gate/high-k oxide interface control.

11.3 — 11:10 a.m.

High Mobility and Excellent Electrical Stability of MOSFETs Using a Novel HfTaO Gate Dielectric, X. Yu, C. Zhu, X.P. Wang, M.F. Li, A. Chin*, A.Y. Du**, W.D. Wang*** and D.-L. Kwong^, National University of Singapore, Singapore, *National Chiao Tung University, Hsinchu, Taiwan, ROC, **Institute of Microelectronics, Singapore, ***Institute of Material Research and Engineering, Singapore, ^University of Texas, Austin, TX

We developed a novel Hf-based gate dielectric for MOSFETs with TaN metal gate. Significant improvements were achieved in contrast to HfO2: (1) crystallization temperature is increased up to 1000ºC; (2) interface states density is reduced by one order of magnitude; (3) electron peak mobility is enhanced by more than two times; (4) threshold voltage shift is reduced by 20 times, greatly prolonging the device lifetime; (5) negligible sub-threshold swing and Gm variations after stress.

11.4 — 11:35 a.m.

Dielectric Breakdown Mechanism of $HfSiON/SiO_2$ Gate Dielectric, K. Torii, T. Aoyama, S. Kamiyama, Y. Tamura, S. Miyazaki*, H. Kitajima and T. Arikado, Semiconductor Leading Edge Technologies, Ibaraki, Japan, *Hiroshima University, Hiroshima, Japan

The breakdown mechanism of HfSiON/SiO2 gate stacks is discussed based on the band diagram, carrier separation and charge pumping measurements. We found that both holes and electrons contribute to breakdown, and that the interfacial layer (IL) thickness is an important parameter. For Vg<0, TBD was determined by IL breakdown. For Vg>0, TBD is controlled by HfSiON bulk breakdown. The situation is more severe in pFET accumulation because of field enhancement due to trapping of holes.